What is claimed is:

1. A solid-state image sensing apparatus comprising:

an image sensing unit in which a plurality of unit cells is laid out on a semiconductor substrate two-dimensionally, each unit cell composing a photoelectric conversion unit operable to convert light into charge and an amplification unit which amplifies an output from the photoelectric conversion unit and outputs an amplified signal;

a plurality of vertical signal lines through which the amplified signals from the unit cells are transmitted in a column direction;

a horizontal direction selection unit operable to select a row of unit cells from the plurality of unit cells laid out in the image sensing region;

a first accumulation capacitor and a second accumulation capacitor which are connected to a vertical signal line for each column and accumulate a signal corresponding to the amplified signal of the unit cell for each row;

an accumulation capacitor selection unit operable to select a capacitor which accumulates the signal from the first accumulation capacitor and the second accumulation capacitor;

a vertical direction selection unit operable to select the first accumulation capacitor and the second accumulation capacitor connected to an arbitrary vertical signal line from the first accumulation capacitors and the second accumulation capacitors connected to each of the plurality of vertical signal lines; and

a horizontal signal line which is connected to a vertical signal line for each column through the vertical direction selection unit and transmits a signal corresponding to the amplified signal accumulated in the first accumulation capacitor or the second accumulation capacitor,

wherein the accumulation capacitor selection unit selects the first accumulation capacitor when a sum of the amplified signals of the unit cells in the plurality of rows is performed, and selects the

second accumulation capacitor when the sum is not performed,

a capacitance of the first accumulation capacitor is smaller than a capacitance of the second accumulation capacitor, and

the capacitance of the second accumulation capacitor is a least capacitance required to read out the signal accumulated in said second accumulation capacitor.

2. The solid-state image sensing apparatus according to Claim 1,

wherein the capacitance of the second accumulation capacitor is a capacitance required to eliminate an external noise from the vertical direction selection unit.

3. The solid-state image sensing apparatus according to Claim2,

wherein the first accumulation capacitor and the second accumulation capacitor are made of n (n is 2 or a larger integer) pieces of third accumulation capacitors connected in parallel, and

the accumulation capacitor selection unit selects: m ($m \leqq n/k$, where m is 1 or a larger integer) pieces of third accumulation capacitors when a sum of the amplified signal of the unit cell in k ($k \leqq n$, where k is 2 or a larger integer) rows is performed; p ($m < p \leqq n$, where p is 2 or a larger integer) pieces of third accumulation capacitors, when the sum is not performed; and all the third capacitors which include signals, when the signals accumulated in the third capacitors are read out.

4. The solid-state image sensing apparatus according to Claim 3,

wherein the accumulation capacitor selection unit selects the third accumulation capacitor k times when the sum is performed, and

the m is the same value in the k times of selection of the third

accumulation capacitor.

5. The solid-state image sensing apparatus according to Claim 4,

wherein the smaller of a total capacitance of the k × m pieces of the third accumulation capacitors and a total capacitance of p pieces of the third accumulation capacitors is larger than predetermined times of a parasitic capacitance of the vertical direction selection unit, and

a value of the predetermined times of the parasitic capacitance is determined by voltage of a signal for a selection by the vertical direction selection unit and voltage of a signal read out from the third accumulation capacitance.

6. The solid-state image sensing apparatus according to Claim 5,

wherein the m is 1, and
the n is equal to the k and the p.

7. The solid-state image sensing apparatus according to Claim 6,

wherein the third accumulation capacitor is connected with the vertical signal line through a clamp capacitor.

8. The solid-state image sensing apparatus according to Claim 7,

wherein the capacitance of the third accumulation capacitor is determined so that an S／N ratio in a case when the sum is performed and an S／N ratio in a case when the sum is not performed are equal.

9. The solid-state image sensing apparatus according to Claim

8,

wherein the capacitance of the third accumulation capacitor is determined by a following equation,

$$Ccp : Csp \fallingdotseq (1-1\sqrt{k}) : (\sqrt{k}-1)$$

where Ccp is a capacitance of a clamp capacitor, Csp is a capacitance of the third accumulation capacitor and k is the number of rows to be summed.

10. The solid-state image sensing apparatus according to Claim 9,

wherein the third accumulation capacitor, the horizontal direction selection unit and the vertical direction selection unit are composed of n-type MOS transistors.

11. The solid-state image sensing apparatus according to Claim 3,

wherein the accumulation capacitor selection unit selects the third accumulation capacitor k times when the sum is performed, and

the m is different value in the k times of selection of the third accumulation capacitor.

12. The solid-state image sensing apparatus according to Claim 11,

wherein the third accumulation capacitor is connected with the vertical signal line through a clamp capacitor.

13. The solid-state image sensing apparatus according to Claim 12,

wherein the capacitance of the third accumulation capacitor is determined so that an S／N ratio in a case when the sum is performed and an S／N ratio in a case when the sum is not

performed are equal.

14. The solid state image sensing apparatus according to Claim 13,

wherein the capacitance of the third accumulation capacitor is determined by a following equation,

$$Ccp : Csp \fallingdotseq (1-1\sqrt{k}) : (\sqrt{k}-1)$$

where Ccp is a capacitance of a clamp capacitor, Csp is a capacitance of the third accumulation capacitor and k is the number of rows to be summed.

15. The solid-state image sensing apparatus according to Claim 14,

wherein the third accumulation capacitor, the horizontal direction selection unit and the vertical direction selection unit are composed of n-type MOS transistors.

16. The solid-state image sensing apparatus according to Claim 3,

wherein the third accumulation capacitor is connected with the vertical signal line through a clamp capacitor.

17. The solid-state image sensing apparatus according to Claim 16,

wherein the capacitance of the third accumulation capacitor is determined so that an S／N ratio in a case when the sum is performed and an S／N ratio in a case when the sum is not performed are equal.

18. The solid-state image sensing apparatus according to Claim 17,

wherein the capacitance of the third accumulation capacitor is

determined by a following equation,

$$Ccp : Csp \fallingdotseq (1-1\sqrt{k}) : (\sqrt{k}-1)$$

where Ccp is a capacitance of a clamp capacitor, Csp is a capacitance of the third accumulation capacitor and k is the number of rows to be summed.

19. The solid-state image sensing apparatus according to Claim 18,

wherein the third accumulation capacitor, the horizontal direction selection unit and the vertical direction selection unit are composed of n-type MOS transistors.

20. The solid-state image sensing apparatus according to Claim 1,

wherein the first accumulation capacitor and the second accumulation capacitor are made of n (n is 2 or a larger integer) pieces of third accumulation capacitors connected in parallel, and

the accumulation capacitor selection unit selects: m ($m \leqq n/k$, where m is 1 or a larger integer) pieces of third accumulation capacitors when a sum of the amplified signal of the unit cell in k ($k \leqq n$, where k is 2 or a larger integer) rows is performed; p ($m < p \leqq n$, where p is 2 or a larger integer) pieces of third accumulation capacitors, when the sum is not performed; and all the third capacitors which include signals, when the signals accumulated in the third capacitors are read out.

21. A driving method for a solid-state image sensing apparatus,

wherein the solid-state image sensing apparatus includes an image sensing region in which a plurality of unit cells is laid out on a semiconductor substrate two-dimensionally, each unit cell composing a photoelectric conversion unit which converts a light signal into signal charge and an amplification unit which amplifies

output of the photoelectric conversion unit and outputs an amplified signal; a plurality of vertical signal lines which transmit the amplified signals of the unit cells in a direction of a column; and a plurality of accumulation capacitors which are connected to a vertical signal line for each column and accumulate signals corresponding to the amplified signals of the unit cells,

when a sum of amplified signals of the unit cells in a plurality of rows is performed, after one accumulation capacitor is selected independently for each row to be summed from the plurality of accumulation capacitors and a signal corresponding to the amplified signal for each row is accumulated, all of accumulation capacitors are selected, each of said accumulation capacitors accumulating the signal corresponding to the amplified signal and

when the sum is not performed, two or more accumulation capacitors which accumulate a signal corresponding to the amplified signal for each row are selected in parallel from the plurality of accumulation capacitors.